REMARKS

Claims 1-51 are pending in the Application. Claims 1, 5, 8, 16, 19, 27, 30, 38, 41 and 49 are rejected under 35 U.S.C. § 102(b). Claims 2-4, 6-7, 9-15, 17, 18, 20-26, 28, 29, 31-37, 39, 40, 42-48, 50 and 51 are rejected under 35 U.S.C. §103(a). Applicants respectfully traverse these rejections for at least the reasons stated below and respectfully request that the Examiner reconsider and withdraw these rejections.

I. REJECTIONS UNDER 35 U.S.C. §102(b):

The Examiner has rejected claims 1, 5, 8, 16, 19, 27, 30, 38, 41 and 49 under 35 U.S.C. §102(b) as being anticipated by Witt et al. (U. S. Patent No. 6,167,506) (hereinafter "Witt"). Applicants respectfully traverse these rejections for at least the reasons stated below and respectfully request the Examiner to reconsider and withdraw these rejections.

For a claim to be anticipated under 35 U.S.C. §102, each and every claim limitation must be found within the cited prior art reference and arranged as required by the claim. M.P.E.P. §2131.

Applicants respectfully assert that Witt does not disclose "calculating n-1 least significant bits of said target address of said branch instruction" as recited in claim 1 and similarly in claims 8, 19, 30 and 41. The Examiner cites Figures 2, 4 and 4A of Witt as well as column 3, line 64 – column 4, line 37; column 21, lines 13-40 and column 23, lines 3-63 of Witt as disclosing the above-cited claim limitation. Paper No. 3, page 2. Applicants respectfully traverse and assert that Witt instead discloses that a plurality of instruction bytes including the relative transfer instruction are predecoded to detect the presence of the relative control transfer instruction. Column 3, line 66 – column 4, line 1. Witt further discloses that an address is added to a displacement included in the relative control transfer instruction, thereby generating the target address. Column 4, lines 1-4. Witt further discloses that the displacement is replaced within the relative control transfer instruction with an encoding indicative of the target address. Column 4, lines 4-6. Witt further discloses that the plurality of instruction bytes including the relative control transfer instruction is stored in an

instruction cache, with the displacement replaced by the encoding. Column 4, lines 6-9. Witt further discloses that the displacements may be any desirable size. Column 21, lines 16-17. Witt further discloses that the displacement encoder receives the target address calculated by an adder and encodes the target address into a format storable into the displacement bytes. Column 23, lines 15-17. Witt further discloses that the displacement stores the entirety of the target address. Column 23, lines 18-19. While Witt discloses adding an address to the displacement to generate a target address and then storing the entire target address in the displacement, there is no language in the cited passages that discloses calculating n-1 least significant bits of a target address of a branch instruction. Thus, Witt does not disclose all of the limitations of claims 1, 8, 19, 30 and 41, and thus Witt does not anticipate claims 1, 8, 19, 30 and 41. M.P.E.P. §2131.

Applicants further assert that Witt does not disclose "replacing n-1 least significant bits of said offset of said target address with said n-1 least significant bits of said target address of said branch instruction" as recited in claim 1 and similarly in claims 8, 19, 30 and 41. The Examiner cites Figures 2, 4 and 4A of Witt as well as column 3, line 64 – column 4, line 37; column 21, lines 13-40 and column 23, lines 3-63 of Witt as disclosing the above-cited claim limitation. Paper No. 3, page 2. Applicants respectfully traverse. As stated above, Witt instead discloses that a plurality of instruction bytes including the relative transfer instruction are predecoded to detect the presence of the relative control transfer instruction. Column 3, line 66 – column 4, line 1. Witt further discloses that an address is added to a displacement included in the relative control transfer instruction, thereby generating the target address. Column 4, lines 1-4. Witt further discloses that the displacement is replaced within the relative control transfer instruction with an encoding indicative of the target address. Column 4, lines 4-6. Witt further discloses that the plurality of instruction bytes including the relative control transfer instruction is stored in an instruction cache, with the displacement replaced by the encoding. Column 4, lines 6-9. Witt further discloses that the displacements may be any desirable size. Column 21, lines 16-17. Witt further discloses that the displacement encoder receives the

target address calculated by an adder and encodes the target address into a format storable into the displacement bytes. Column 23, lines 15-17. Witt further discloses that the displacement stores the entirety of the target address. Column 23, lines 18-19. While Witt discloses adding an address to the displacement to generate a target address and then storing the entire target address in the displacement, there is no language in the cited passages that discloses replacing n-1 least significant bits of an offset of a target address with n-1 least significant bits of a target address of a branch instruction. Thus, Witt does not disclose all of the limitations of claims 1, 8, 19, 30 and 41, and thus Witt does not anticipate claims 1, 8, 19, 30 and 41. M.P.E.P. §2131.

Claims 5, 16, 27, 38 and 49 each recite combinations of features including the above combinations, and thus are not anticipated for at least the above-stated reasons. Claims 5, 16, 27, 38 and 49 recite additional features which, in combination with the features of the claims upon which they depend, are not anticipated by Witt.

For example, Witt does not disclose "adding a value stored in said n-1 least significant bits of said offset of said target address stored in said branch instruction with a value stored in said n-1 least significant bits of said address of said branch instruction" as recited in claim 5 and similarly in claims 16, 27, 38 and 49. The Examiner cites column 22, lines 4-30 of Witt as disclosing the above-cited claim limitation. Paper No. 3, page 3. Applicants respectfully traverse and assert that Witt instead discloses that responsive to the signal from a byte predecoder indicating that a relative branch instruction has been detected, a control unit causes a target generator to generate the target address corresponding to the relative branch instruction. Column 22, lines 4-8. Witt further discloses that the displacement byte or bytes are selected from the instruction bytes stored in a register. Column 22, lines 8-9. Witt further discloses that additionally, the fetch address stored in a fetch address register is provided to the target generator. Column 22, lines 9-13. Witt further discloses that the target generator adds the received address and displacement byte or bytes, thereby generating the target address. Column 22, lines 13-15. Witt further discloses that the generated target address is then encoded for storage as a replacement for the

displacement field of the relative branch instruction. Column 22, lines 15-17. While Witt discloses that the target generator adds the address stored in the fetch address register with the displacement to generate the target address, there is no language in the cited passage that discloses that the target generator adds a value stored in the n-1 least significant bits of an offset of a target address with a value stored in the n-1 least significant bits of an address of a branch instruction. Thus, Witt does not disclose all of the limitations of claims 5, 16, 27, 38 and 49, and thus Witt does not anticipate claims 5, 16, 27, 38 and 49. M.P.E.P. §2131.

As a result of the foregoing, Applicants respectfully assert that not each and every claim limitation was found within Witt, and thus claims 1, 5, 8, 16, 19, 27, 30, 38, 41 and 49 are not anticipated by Witt. M.P.E.P. §2131.

II. REJECTIONS UNDER 35 U.S.C. §103(a):

The Examiner has rejected claims 2-4, 6-7, 9-15, 17, 18, 20-26, 28, 29, 31-37, 39, 40, 42-48, 50 and 51 under 35 U.S.C. §103(a) as being unpatentable over Witt in view of Boutaud et al. (U.S. Patent No. 5,907,714) (hereinafter "Boutaud"). Applicants respectfully traverse these rejections for at least the reasons stated below and respectfully request the Examiner to reconsider and withdraw these rejections.

A. The Examiner has not provided any objective evidence for combining Witt with Boutaud.

A *prima facie* showing of obviousness requires the Examiner to establish, *inter alia*, that the prior art references teach or suggest, either alone or in combination, all of the limitations of the claimed invention, and the Examiner must provide a motivation or suggestion to combine or modify the prior art reference to make the claimed inventions. M.P.E.P. §2142. The showings must be clear and particular and supported by objective evidence. *In re Lee*, 277 F.3d 1338, 1343, 61 U.S.P.Q.2d 1430, 1433-34 (Fed. Cir. 2002); *In re Kotzab*, 217 F.3d 1365, 1370, 55 U.S.P.Q.2d 1313, 1317 (Fed. Cir. 2000); *In re Dembiczak*, 50 U.S.P.Q.2d. 1614, 1617 (Fed. Cir. 1999). Broad conclusory statements regarding the teaching of multiple references, standing alone, are not evidence. *Id.*

The Examiner's motivation for modifying Witt with Boutaud to append a carry bit to a branch instruction thereby increasing a length of the branch instruction by one bit, as recited in claim 2 and similarly in claims 9, 20, 31 and 42, is "to provide a more efficient way to test for branch status condition since the condition bit would have been readily available." Paper No. 3, page 3. The Examiner's motivation is insufficient to support a *prima facie* case of obviousness for at least the reasons stated below.

The motivation to modify Witt with Boutaud must come from one of three possible sources: the nature of the problem to be solved, the teachings of the prior art, and the knowledge of persons of ordinary skill in the art. *In re Rouffet*, 149 F.3d 1350, 1357, 47 U.S.P.Q.2d 1453, 1457-58 (Fed. Cir. 1998). The Examiner has not provided any evidence that his motivation comes from any of these sources. Instead, the Examiner is relying upon his own subjective opinion which is insufficient to support a *prima facie* case of obviousness. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002). Consequently, the Examiner's motivation is insufficient to support a *prima facie* case of obviousness for rejecting claims 2-4, 6-7, 9-15, 17, 18, 20-26, 28, 29, 31-37, 39, 409, 42-48, 50 and 51.

Furthermore, the Examiner's motivation is not a motivation as to why one of ordinary skill in the art with the primary reference (Witt) in front of him would have been motivated to modify the primary reference (Witt) with the teachings of the secondary reference (Boutaud). That is, the Examiner's motivation does not address as to why one of ordinary skill in the art would modify Witt to append a carry bit to a branch instruction thereby increasing a length of the branch instruction by one bit (Examiner admits that Witt does not teach this limitation). The Examiner has not explained how providing a more efficient way to test for branch status condition (Examiner's motivation) is related to appending a carry bit to a branch instruction thereby increasing a length of the branch instruction by one bit. Instead, the Examiner is merely relying upon his own subjective opinion which is insufficient to support a *prima facie* case of obviousness. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed.

Cir. 2002). Consequently, the Examiner's motivation is insufficient to support a *prima facie* case of obviousness for rejecting claims 2-4, 6-7, 9-15, 17, 18, 20-26, 28, 29, 31-37, 39, 409, 42-48, 50 and 51.

Furthermore, the Examiner has not provided a motivation for modifying Witt to have a set of upper order bit value combinations of an address of a branch instruction that comprises one or more of the following: a value in the upper order bits of the address of the branch instruction incremented by one, the value in the upper order bits of the address of the branch instruction decremented by one and the value in the upper order bits of the address of the branch instruction, as recited in claim 6 and similarly in claims 17, 28, 39 and 50. Neither has the Examiner provided a motivation for modifying Witt to have one of the set of upper order bit value combinations be selected in response to a value in a sign bit and a value in the carry bit in the branch instruction, as recited in claim 7 and similarly in claims 18, 29, 40 and 51. In order to establish a *prima facie* case of obviousness, the Examiner must provide a motivation to modify Witt as indicated above. M.P.E.P. §2142. The Examiner has not provided any such motivation but instead relies upon his own subjective opinion which is insufficient to establish a *prima facie* case of obviousness. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002). Consequently, the Examiner has not presented a *prima facie* case of obviousness in rejecting claims 6, 7, 17, 18, 28, 29, 39, 40, 50 and 51. *Id.*

Further, the Examiner must submit objective evidence and not rely on his own subjective opinion in support of combining Witt, which teaches replacing the displacement field of a relative branch instruction with an encoding of the target address (Abstract of Witt), with Boutaud, which teaches a circuit having status conditions where a particular set of the status conditions can occur in operation of the circuit (Abstract of Boutaud). *Id.* There is no suggestion in Witt of having status conditions. Neither is there any suggestion in Witt of having a particular set of the status conditions occur in the operation of a circuit. Since the Examiner has not submitted objective evidence for modifying Witt with Boutaud, the Examiner has not

presented a *prima facie* case of obviousness for rejecting claims 2-4, 6-7, 9-15, 17, 18, 20-26, 28, 29, 31-37, 39, 409, 42-48, 50 and 51. *Id.*

Further, the Examiner must submit objective evidence and not rely on his own subjective opinion in support of modifying Witt to append a carry bit to a branch instruction thereby increasing a length of the branch instruction by one bit (Examiner admits that Witt does not teach this limitation). *Id.* There is no suggestion in the nature of the problem to be solved, the teachings of Witt and Boutaud, and the knowledge of persons of ordinary skill in the art to append a carry bit to a branch instruction. Neither is there any suggestion in the nature of the problem to be solved, the teachings of Witt and Boutaud, and the knowledge of persons of ordinary skill in the art to append a carry bit to a branch instruction thereby increasing a length of the branch instruction by one bit. Since the Examiner has not submitted objective evidence for modifying Witt to append a carry bit to a branch instruction thereby increasing a length of the branch instruction by one bit, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 2-4, 6-7, 9-15, 17, 18, 20-26, 28, 29, 31-37, 39, 409, 42-48, 50 and 51. *Id.*

Further, the Examiner must submit objective evidence and not rely on his own subjective opinion in support of modifying Witt to have a set of upper order bit value combinations of an address of a branch instruction that comprises one or more of the following: a value in the upper order bits of the address of the branch instruction incremented by one, the value in the upper order bits of the address of the branch instruction decremented by one and the value in the upper order bits of the address of the branch instruction (Examiner admits that Witt does not teach this limitation). *Id.* There is no suggestion in the nature of the problem to be solved, the teachings of Witt and Boutaud, and the knowledge of persons of ordinary skill in the art of having a set of upper order bit value combinations of an address of a branch instruction. Neither is there any suggestion in the nature of the problem to be solved, the teachings of Witt and Boutaud, and the knowledge of persons of ordinary skill in the art of having a set of upper order bit value combinations of an address of a branch instruction that

comprises one or more of the following: a value in the upper order bits of the address of the branch instruction incremented by one, the value in the upper order bits of the address of the branch instruction decremented by one and the value in the upper order bits of the address of the branch instruction. Since the Examiner has not submitted objective evidence for modifying Witt to have a set of upper order bit value combinations of an address of a branch instruction that comprises one or more of the following: a value in the upper order bits of the address of the branch instruction incremented by one, the value in the upper order bits of the address of the branch instruction decremented by one and the value in the upper order bits of the address of the branch instruction, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 6, 17, 28, 39 and 50. *Id.*

Further, the Examiner must submit objective evidence and not rely on his own subjective opinion in support of modifying Witt to have one of the set of upper order bit value combinations be selected in response to a value in a sign bit and a value in the carry bit in the branch instruction (Examiner admits that Witt does not teach this limitation). *Id.* There is no suggestion in the nature of the problem to be solved, the teachings of Witt and Boutaud, and the knowledge of persons of ordinary skill in the art of having one of the set of upper order bit value combinations be selected in response to a value in a sign bit. Neither is there any suggestion in the nature of the problem to be solved, the teachings of Witt and Boutaud, and the knowledge of persons of ordinary skill in the art of having one of the set of upper order bit value combinations be selected in response to a value in the carry bit in the branch instruction. Since the Examiner has not submitted objective evidence for modifying Witt to have one of the set of upper order bit value combinations be selected in response to a value in a sign bit and a value in the carry bit in the branch instruction, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 7, 18, 29, 40 and 51. *Id.*

As a result of the foregoing, Applicants respectfully assert that the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 2-4, 6-7, 9-15, 17, 18, 20-26, 28, 29, 31-37, 39, 409, 42-48, 50 and 51. M.P.E.P. §2143.

B. By combining Witt with Boutaud, the principle of operation of Witt would change.

If the proposed modification or combination of the prior art would change the principle of the operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. *In re Ratti*, 270 F.2d 810, 123 U.S.P.Q. 349 (C.C.P.A. 1959). Further, if the proposed modification would render the prior art invention being modified unsatisfactorily for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 U.S.P.Q. 1125 (Fed. Cir. 1984). For the reasons discussed below, Applicants submit that by combining Witt with Boutaud, the principle of operation in Witt would change and subsequently render the operation of Witt to perform its purpose unsatisfactorily.

Witt teaches a processor configured to predecode instruction bytes prior to their storage within an instruction cache. Column 3, lines 1-2. Witt further teaches that during the predecoding, relative branch instructions are detected. Column 3, lines 2-3. Witt further teaches that the displacement included within the relative branch instruction is added to the address corresponding to the relative branch instruction, thereby generating the target address. Column 3, lines 3-6. Witt further teaches that the processor replaces the displacement field of the relative branch instruction with an encoding of the target address, and stores the modified relative branch instruction in the instruction cache. Column 3, lines 6-10. Witt further teaches that advantageously, the branch prediction mechanism employed by the processor may more rapidly generate the target address corresponding to relative branch instructions. Column 3, lines 10-12. Witt further teaches that the branch prediction mechanism may simply select the target address from the displacement field of the relative branch instruction instead of performing an addition to generate the target address. Column 3, lines 13-

16. Witt further teaches that the rapidly generated target address may be provided to the instruction cache for fetching instructions more quickly than might otherwise be achieved. Column 3, lines 16-19. Witt further teaches that the amount of time elapsing between fetching a branch instruction and generating the corresponding target address may advantageously be reduced. Column 3, lines 19-21. Witt further teaches that accordingly, the branch prediction mechanism may operate more efficiently, and hence processor performance may be increased through more rapid fetching of instructions stored at the target address. Column 3, lines 21-25.

Boutaud, on the other hand, teaches a circuit having status conditions where a particular set of the status conditions can occur in operation of the circuit. Column 3, lines 3-5. Boutaud further teaches an instruction register that holds a branch instruction conditional on a particular set of the status conditions. Column 3, lines 5-7. Boutaud further teaches a decoder that is connected to the instruction register and the circuit. Column 3, lines 7-8. Boutaud further teaches a program counter that is coupled to the decoder where the decoder is operable to enter a branch address into the program counter in response to the branch instruction when the particular set of the status conditions of the circuit are present. Column 3, lines 8-12.

By combining Witt with Boutaud, Witt would no longer be able to reduce the amount of time elapsing between fetching a branch instruction and generating the corresponding target address. There is no language in Boutaud that teaches generating target addresses, predecoding instructions, detecting branch instructions or having a displacement field in a branch instruction. Instead, Witt would be modified to have a circuit with status conditions where a register in the circuit would hold a branch instruction conditional on a particular set of the status conditions. Since the conditional branch instruction has no displacement field, Witt would no longer be able to add the displacement within the conditional branch instruction to an address corresponding to the conditional branch instruction, thereby generating the target address. Consequently, by combining Witt with Boutaud, Witt would no longer be capable of generating a target address such as by adding the displacement to the

address corresponding to the relative branch instruction. Hence, Witt would not be able to reduce the amount of time elapsing between fetching a branch instruction and generating the corresponding target address. Thus, by combining Witt with Boutaud, the principle of operation in Witt would change, and subsequently render the operation of Witt to perform its purpose unsatisfactorily. Therefore, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 2-4, 6-7, 9-15, 17, 18, 20-26, 28, 29, 31-37, 39, 409, 42-48, 50 and 51. *In re Ratti*, 270 F.2d 810, 123 U.S.P.Q. 349 (C.C.P.A. 1959); *In re Gordon*, 733 F.2d 900, 221 U.S.P.Q. 1125 (Fed. Cir. 1984).

C. The Examiner has not presented a reasonable expectation of success when combining Witt with Boutaud.

The Examiner must present a reasonable expectation of success in combining Witt with Boutaud in order to establish a *prima facie* case of obviousness. M.P.E.P. §2143.02.

As stated above, Witt teaches a processor configured to predecode instruction bytes prior to their storage within an instruction cache. Column 3, lines 1-2. Witt further teaches that during the predecoding, relative branch instructions are detected. Column 3, lines 2-3. Witt further teaches that the displacement included within the relative branch instruction is added to the address corresponding to the relative branch instruction, thereby generating the target address. Column 3, lines 3-6. Witt further teaches that the processor replaces the displacement field of the relative branch instruction with an encoding of the target address, and stores the modified relative branch instruction in the instruction cache. Column 3, lines 6-10.

As stated above, Boutaud, on the other hand, teaches a circuit having status conditions where a particular set of the status conditions can occur in operation of the circuit. Column 3, lines 3-5. Boutaud further teaches an instruction register that holds a branch instruction conditional on a particular set of the status conditions. Column 3, lines 5-7. Boutaud further teaches a decoder that is connected to the instruction register and the circuit. Column 3, lines 7-8. Boutaud further teaches a program

counter that is coupled to the decoder where the decoder is operable to enter a branch address into the program counter in response to the branch instruction when the particular set of the status conditions of the circuit are present. Column 3, lines 8-12.

The Examiner has not presented any evidence that there would be a reasonable expectation of success in combining Witt, that relates to generating a target address by adding the displacement included within the relative branch to the address corresponding to the relative branch instruction, with Boutaud, that relates to having a circuit with status conditions where a register in the circuit would hold a branch instruction conditional on a particular set of the status conditions. The Examiner must provide objective evidence as to how generating a target address by adding the displacement included within the relative branch to the address corresponding to the relative branch instruction would be combined with a circuit having status conditions where a register in the circuit would hold a branch instruction conditional on a particular set of the status conditions. M.P.E.P. §2143.02. Since the Examiner has not provided such evidence, the Examiner has not presented a reasonable expectation of success in combining Witt with Boutaud. M.P.E.P. §2143.02. Accordingly, the Examiner has not presented a *prima facie* case of obviousness in rejecting claims 2-4, 6-7, 9-15, 17, 18, 20-26, 28, 29, 31-37, 39, 409, 42-48, 50 and 51. M.P.E.P. §2143.02.

D. Witt and Boutaud, taken singly or in combination, do not teach or suggest the following limitations.

Applicants respectfully assert that Witt and Boutaud, taken singly or in combination, do not teach or suggest "appending a carry bit to said branch instruction thereby increasing a length of said branch instruction by one bit" as recited in claim 2 and similarly in claims 9, 20, 31 and 42. The Examiner cites Figures 31, 32 and 35 of Boutaud as well as column 46, lines 5-46 of Boutaud as teaching the above-cited claim limitation. Paper No. 3, page 3. Applicants respectfully traverse and assert that Boutaud instead teaches a circuit that has status conditions where a particular set of status conditions can occur in operation of the circuit. Column 46, lines 6-8.

Boutaud further teaches an instruction register that holds a conditional branch instruction that is conditional on a particular set of the status conditions. Column 46, lines 8-10. Boutaud further teaches that a branch address is entered into the program counter when the particular set of the status conditions of the circuit are present. Column 46, lines 13-16. Boutaud further teaches that the status conditions may include a carry bit. Column 46, lines 32-34. However, there is no language in Boutaud that teaches appending a carry bit to a branch instruction. Neither is there any language in Boutaud that teaches appending a carry bit to a branch instruction thereby increasing a length of the branch instruction by one bit. Therefore, the Examiner has not presented a *prima facie* case of obviousness in rejecting claims 2, 9, 20, 31 and 42, since the Examiner is relying upon an incorrect, factual predicate in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

Applicants further assert that Witt and Boutaud, taken singly or in combination, do not teach or suggest "calculating a set of upper order bit value combinations of an address of said branch instruction; storing said branch instruction storing said n-1 least significant bits of said target address in a cache; retrieving said branch instruction storing said n-1 least significant bits of said target address from said cache; and selecting a one of said set of upper order bit value combinations of said address of said branch instruction" as recited in claim 3 and similarly in claims 10-14, 21-25, 32-36 and 43-47. The Examiner cites column 22, lines 40-65 and column 23, lines 15-41 of Witt as teaching the above-cited claim limitations. Paper No. 3, page 4. Applicants respectfully traverse.

Witt instead teaches that if a relative branch instruction spans the boundary between two cache lines, the predecode unit may be configured to fetch the succeeding cache line in order to complete the predecoding for the relative branch instruction. Column 22, lines 40-46. Witt further teaches an embodiment of a target generator. Column 22, lines 49-65. Witt further teaches a displacement encoder receives a target address calculated by an adder and encodes the target address into a format storable into the displacement bytes. Column 23, lines 15-17. Witt further

teaches that the displacement stores the entirety of the target address. Column 23, lines 17-19. Witt further teaches that a portion of the displacement byte is used to store the offset of the target address within the target cache line. Column 23, lines 24-26. Witt further teaches that the remaining portion of the displacement byte and the corresponding control transfer bit is encoded with a value indicating the target cache line as a number of cache lines above or below the cache line identified by the fetch address stored in the fetch address register. Column 23, lines 27-32. There is no language in the cited passages that teaches calculating a set of upper order bit value combinations of an address of a branch instruction. Neither is there any language in the cited passages that teaches storing a branch instruction storing n-1 least significant bits of a target address in a cache. Neither is there any language in the cited passages that teaches retrieving a branch instruction storing n-1 least significant bits of a target address from a cache. Neither is there any language in the cited passages that teaches selecting one of the set of upper order bit value combinations of the address of the branch instruction. Therefore, the Examiner has not presented a *prima facie* case of obviousness in rejecting claims 3, 10-14, 21-25, 32-36 and 43-47, since the Examiner is relying upon an incorrect, factual predicate in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

Applicants further assert that Witt and Boutaud, taken singly or in combination, do not teach or suggest "appending said selected one of said set of upper order bit value combinations of said address of said branch instruction with said n-1 least significant bits of said target address to calculate said target address of said branch instruction" as recited in claim 4 and similarly in claims 15, 26, 37 and 48. The Examiner cites column 22, lines 49-65 of Witt as teaching the above-cited claim limitation. Paper No. 3, page 4. Applicants respectfully traverse and assert that Witt instead teaches an embodiment of a target generator. Column 22, lines 49-65. There is no language in the cited passage that teaches appending a selected one of a set of upper order bit value combinations of an address of a branch instruction with n-1 least significant bits of a target address. Neither is there any language in the cited passages

that teaches appending a selected one of a set of upper order bit value combinations of an address of a branch instruction with n-1 least significant bits of a target address to calculate the target address of the branch instruction. Therefore, the Examiner has not presented a *prima facie* case of obviousness in rejecting claims 4, 15, 26, 37 and 48, since the Examiner is relying upon an incorrect, factual predicate in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

Applicants further assert that Witt and Boutaud, taken singly or in combination, do not teach or suggest "wherein said set of upper order bit value combinations of said address of said branch instruction comprises one or more of the following: a value in said upper order bits of said address of said branch instruction incremented by one, said value in said upper order bits of said address of said branch instruction decremented by one and said value in said upper order bits of said address of said branch instruction" as recited in claim 6 and similarly in claims 17, 28, 39 and 50. The Examiner states that one of ordinary skill would have motivated to modify Witt to include these limitations. Paper No. 3, page 4. The Examiner further cites column 3, line 28 – column 4, line 36. Paper No. 3, page 4. Applicants respectfully point out that the Examiner has not indicated whether the cited passage is from Witt or Boutaud. Applicants will assume that the cited passage is from Witt. Further, Applicants are assuming that the Examiner is citing this passage from Witt as support for the assertion that Witt in essence teaches the above-cited claim limitations. Based on Applicants understanding as outlined above, Applicants respectfully traverse.

Witt instead teaches that a plurality of instruction bytes including the relative transfer instruction are predecoded to detect the presence of the relative control transfer instruction. Column 3, line 66 – column 4, line 1. Witt further teaches that an address is added to a displacement included in the relative control transfer instruction, thereby generating the target address. Column 4, lines 1-4. Witt further teaches that the displacement is replaced within the relative control transfer instruction with an encoding indicative of the target address. Column 4, lines 4-6. Witt further teaches that the plurality of instruction bytes including the relative control transfer instruction

is stored in an instruction cache, with the displacement replaced by the encoding. Column 4, lines 6-9. There is no language in the cited passage that teaches a set of upper order bit value combinations of an address of a branch instruction. Neither is there any language in the cited passage that teaches a value in the upper order bits of an address of a branch instruction incremented by one. Neither is there any language in the cited passage that teaches a value in the upper order bits of an address of a branch instruction decremented by one. Neither is there any language in the cited passage that teaches a value in the upper order bits of an address of the branch instruction. Therefore, the Examiner has not presented a *prima facie* case of obviousness in rejecting claims 6, 17, 28, 39 and 50, since the Examiner is relying upon an incorrect, factual predicate in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

Applicants further assert that Witt and Boutaud, taken singly or in combination, do not teach or suggest "wherein said one of said set of upper order bit value combinations is selected in response to a value in a sign bit and a value in said carry bit in said branch instruction" as recited in claim 7 and similarly in claims 18, 29, 40 and 51. The Examiner states that one of ordinary skill would have motivated to modify Witt to include this limitation. Paper No. 3, page 4. The Examiner further cites Figures 34 and 35 of Boutaud as well as column 46, lines 5-46 of Boutaud. Paper No. 3, page 4. Applicants are assuming that the Examiner is citing this passage from Boutaud as support for the assertion that Boutaud in essence teaches the above-cited claim limitations. Based on Applicants understanding as outlined above, Applicants respectfully traverse.

Boutaud instead teaches a circuit that has status conditions where a particular set of status conditions can occur in operation of the circuit. Column 46, lines 6-8. Boutaud further teaches an instruction register that holds a conditional branch instruction that is conditional on a particular set of the status conditions. Column 46, lines 8-10. Boutaud further teaches that a branch address is entered into the program counter when the particular set of the status conditions of the circuit are present.

Column 46, lines 13-16. Boutaud further teaches that the status conditions may include a carry bit. Column 46, lines 32-34. However, there is no language in Boutaud that teaches a set of upper order bit value combinations. Neither is there any language in Boutaud that teaches selecting one of the set of upper order bit value combinations. Neither is there any language in Boutaud that teaches selecting one of the set of upper order bit value combinations in response to a value in a sign bit. Neither is there any language in Boutaud that teaches selecting one of the set of upper order bit value combinations in response to a value in a carry bit in a branch instruction. Therefore, the Examiner has not presented a *prima facie* case of obviousness in rejecting claims 7, 18, 29, 40 and 51, since the Examiner is relying upon an incorrect, factual predicate in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

As a result of the foregoing, Applicants respectfully assert that there are numerous claim limitations not taught or suggested in the cited prior art, and thus the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 2-4, 6-7, 9-15, 17, 18, 20-26, 28, 29, 31-37, 39, 40, 42-48, 50 and 51.

III. CONCLUSION

As a result of the foregoing, it is asserted by Applicants that claims 1-51 in the Application are in condition for allowance, and Applicants respectfully request an allowance of such claims. Applicants respectfully request that the Examiner call Applicants' attorney at the below listed number if the Examiner believes that such a discussion would be helpful in resolving any remaining issues.

Respectfully submitted,

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